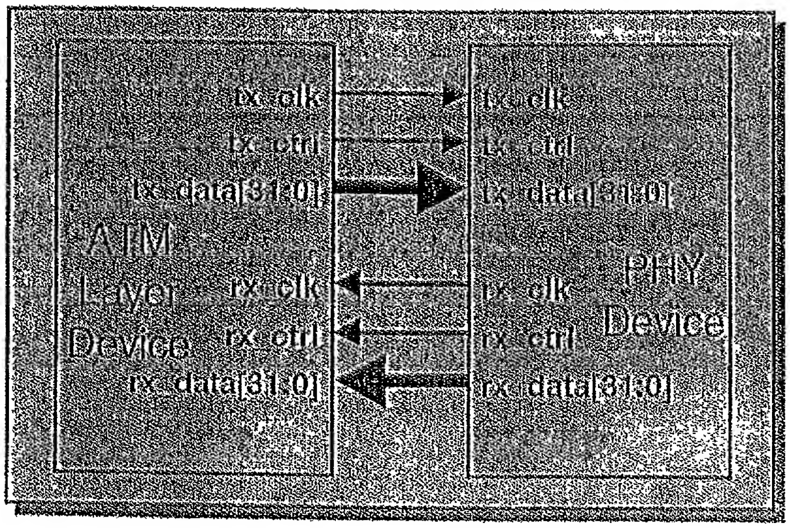
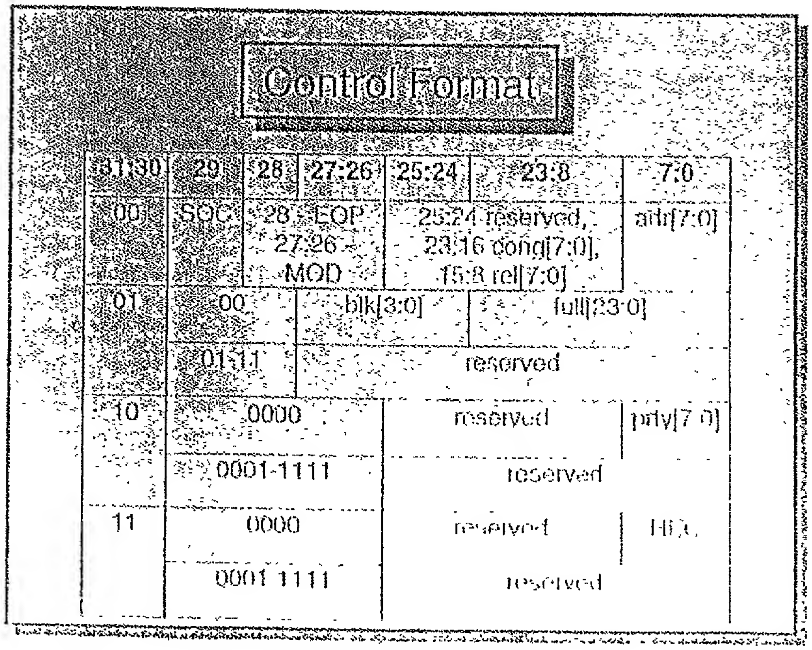
Fig. 1



PRIOR ART

Fig. 2

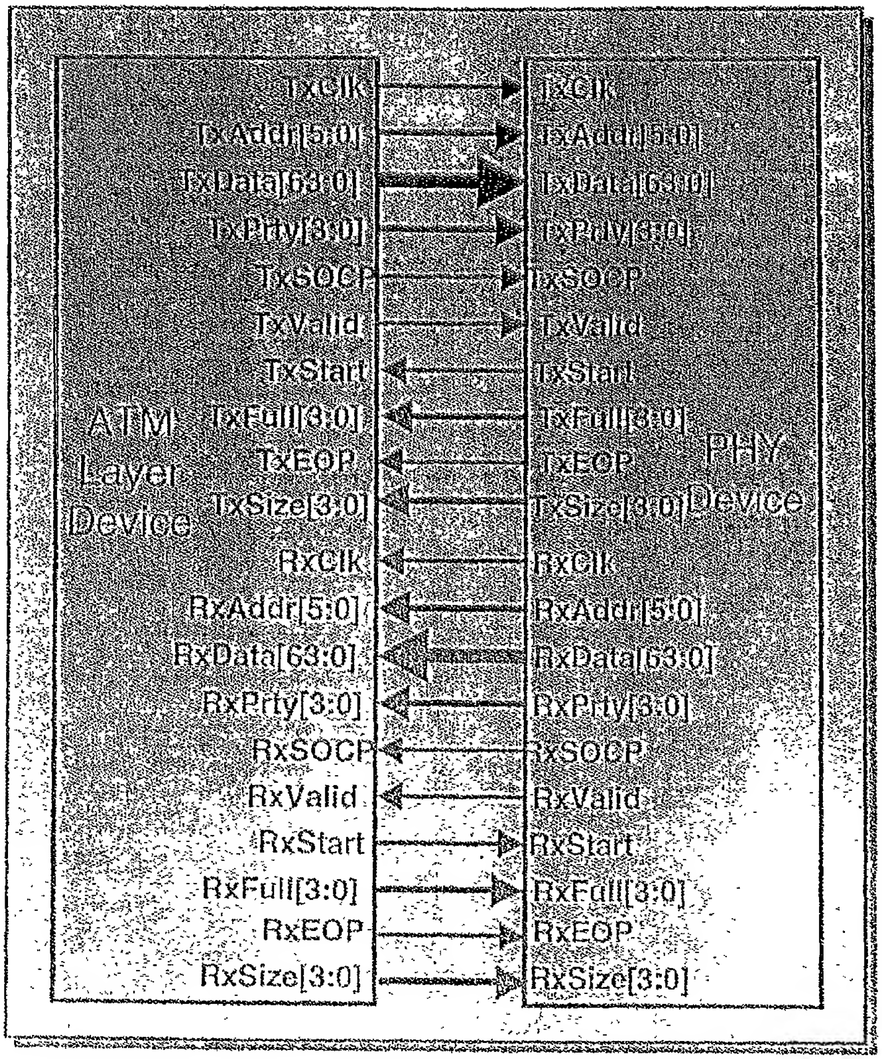


Control Format

31:30	29	28	27:26	25:24	23:8	7:0
00	SOC	28 – EOP 27:26 – MOD		25:24 reserved, 23:16 cong[7:0], 15:8 rel[7:0]		adr[7:0]
01	00		blk[3:0]		full[23:0]	
	01-11		reserved			
10	0000			reserved		prty[7:0]
	0001-1111			reserved		
11	0000			reserved		HEC
	0001-1111			reserved		

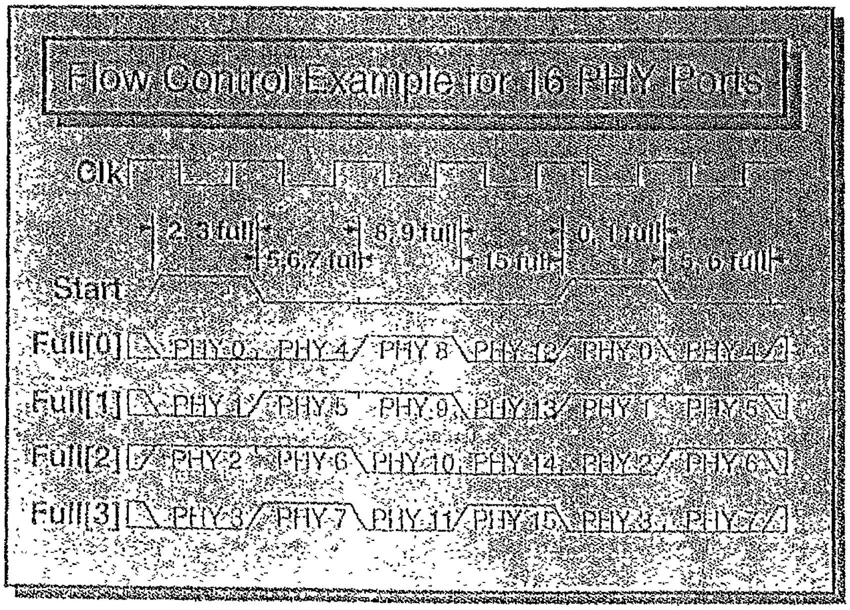
PRIOR ART

Fig. 3



PRIOR ART

Fig. 4.



PRIOR ART

Fig. 5

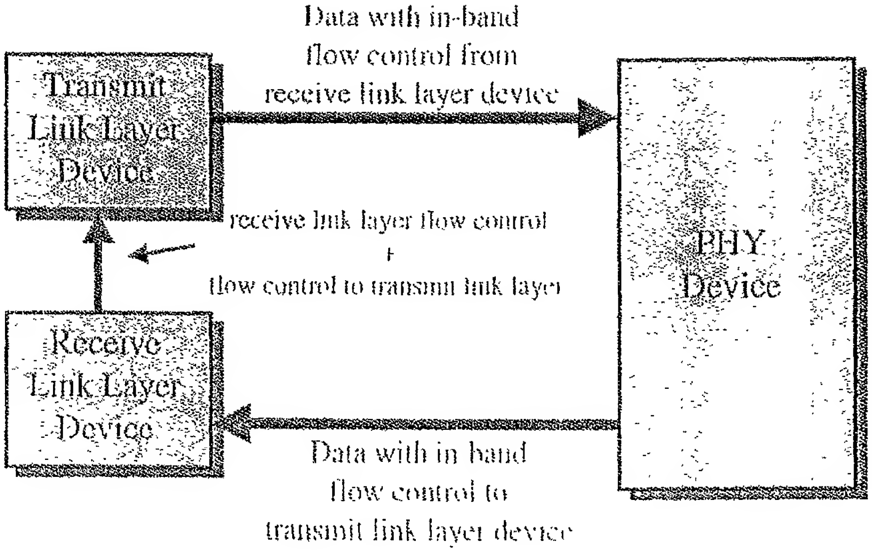
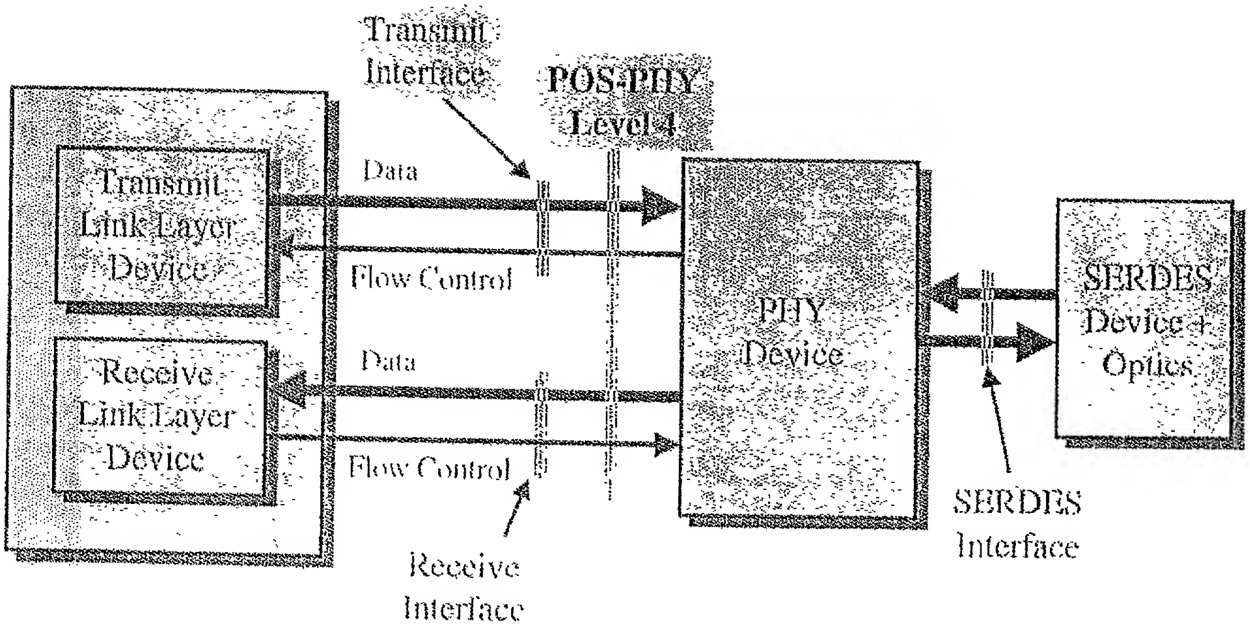

Transmit Link Layer Device
Data with in-band flow control from receive link layer device
receive link layer flow control + flow control to transmit link layer
Receive Link Layer Device
PHY Device
Data with in band flow control to transmit link layer device

Fig. 6



Transmit Interface
POS-PHY Level 4
Transmit Link Layer Device
Data
Flow Control
Receive Link Layer Device
Data
Flow Control
PHY Device
SERDES Device + Optics
SERDES Interface
Receive Interface

FIG. 7

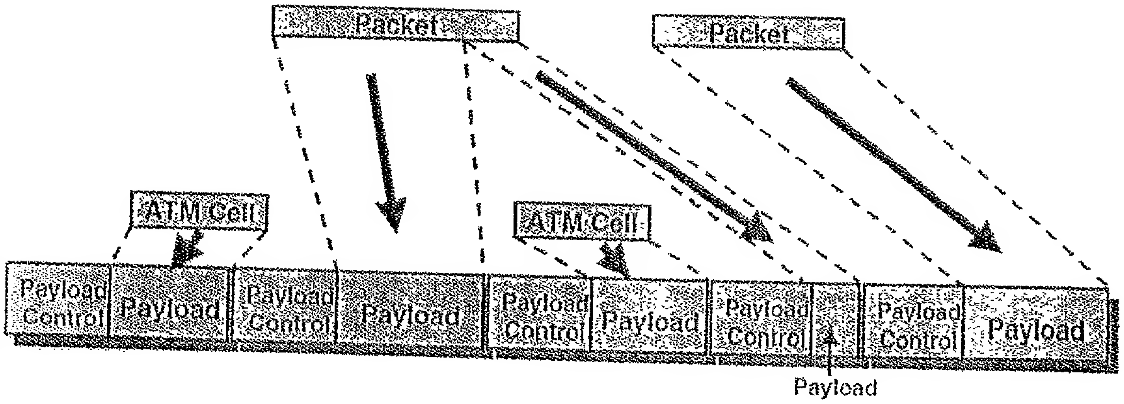

Packet
Packet
ATM Cell
ATM Cell
Payload Control
Payload
Payload Control
Payload
Payload Control
Payload
Payload Control
Payload Control
Payload
Payload

FIG 8

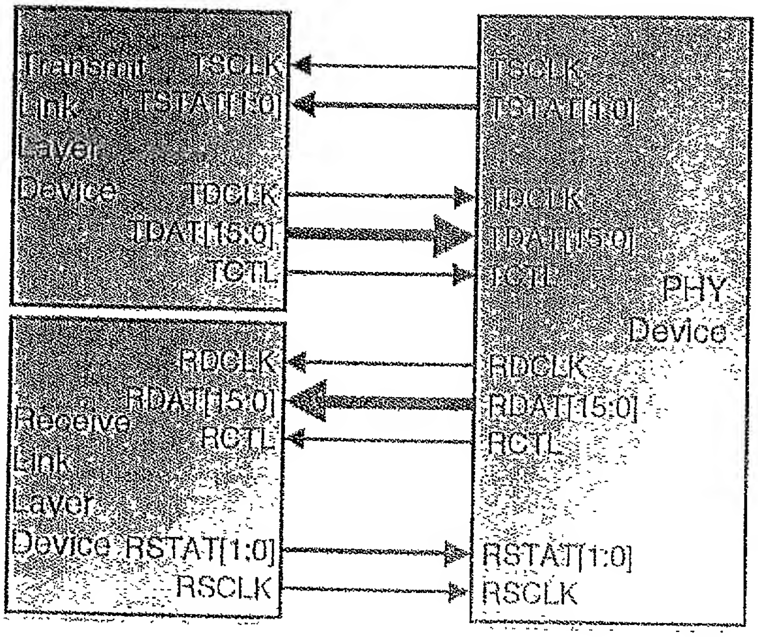
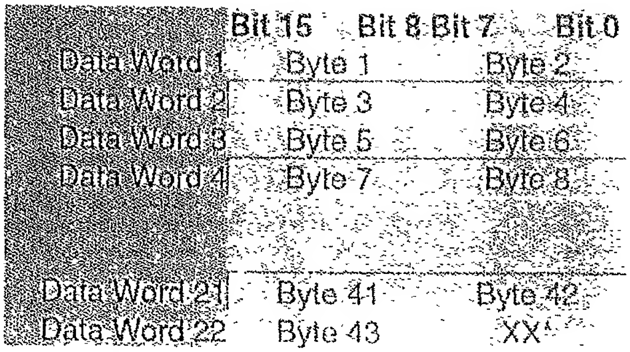

Transmit Link Layer Device
TSCLK
TSTAT[1:0]
TDCLK
TDAT[15:0]
TCTL
Receive Link Layer Device
RDCLK
RDAT[15:0]
RCTL
RSTAT[1:0]
RSCLK
TSCLK
TSTAT[1:0]
TDCLK
TDAT[15:0]
TCTL
PHY Device
RDCLK
RDAT[15:0]
RCTL
RSTAT[1:0]
RSCLK

FIG. 9



	Bit 15 Bit 8	Bit 7 Bit 0
Data Word 1	Byte 1	Byte 2
Data Word 2	Byte 3	Byte 4
Data Word 3	Byte 5	Byte 6
Data Word 4	Byte 7	Byte 8
Data Word 21	Byte 41	Byte 42
Data Word 22	Byte 43	XX

FIG. 10

	Bit 15 Bit 8	Bit 7 Bit 0
Data Word 1	H1	H2
Data Word 2	H3	H4
Data Word 3	P1	P2
Data Word 4	P3	P4
Data Word 25	P45	P46
Data Word 26	P47	P48

FIG. 11

	Bit 15 Bit 8	Bit 7 Bit 0
Data Word 1	H1	H2
Data Word 2	H3	H4
Data Word 3	HEC	UDF
Data Word 4	P1	P2
Data Word 5	P3	P4
Data Word 26	P45	P46
Data Word 27	P47	P48

FIG. 12

	Bit 15 Bit 8	Bit 7 Bit 0
Data Word 1	Extended Address	
Data Word 2	Byte 1	Byte 2
Data Word 3	Byte 3	Byte 4
Data Word 4	Byte 5	Byte 6

FIG. 13

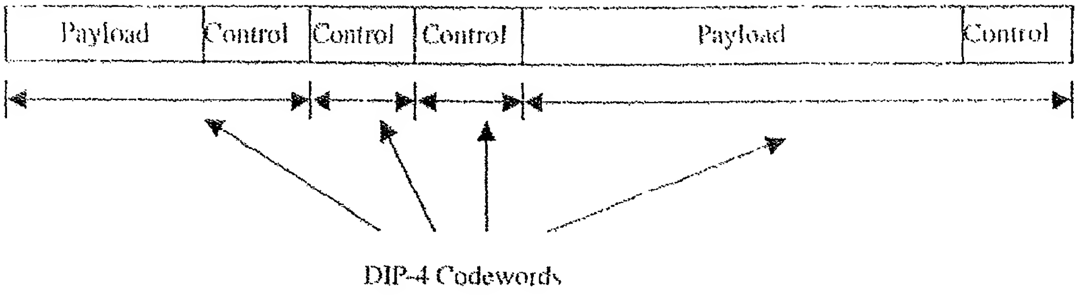

Payload
Control
Control
Control
Payload
Control
DIP-4 Codewords

FIG. 14

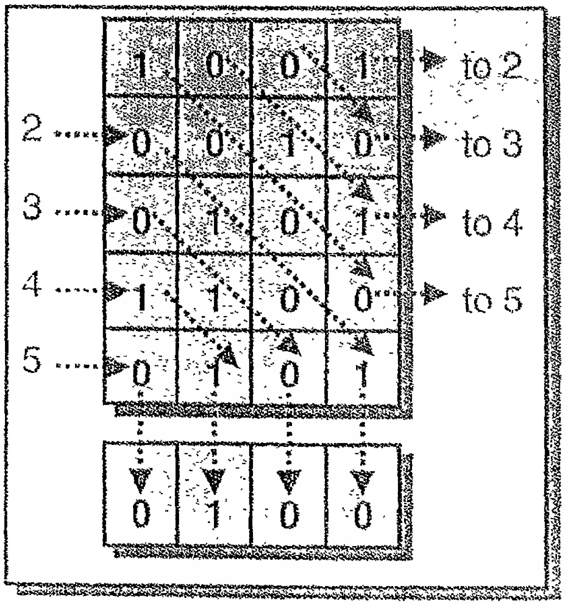

1 0 0 1
to 2
2
0 0 1 0
to 3
3
0 1 0 1
to 4
4
1 1 0 0
to 5
5
0 1 0 1
0 1 0 0

FIG. 15

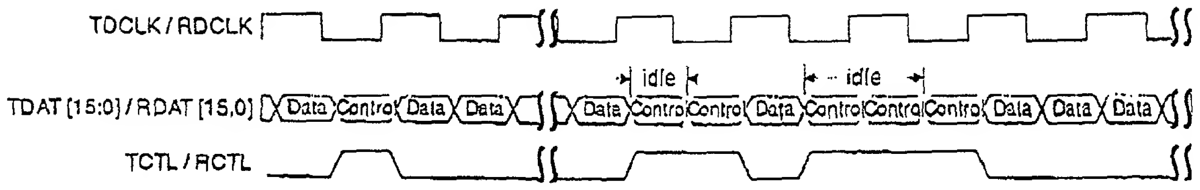

TDCLK / RDCLK
TDAT [15:0] / RDAT [15,0]
TCTL / RCTL
idle
idle
Data
Control
Data
Data
Data
Control
Control
Data
Control
Control
Control
Data
Data
Data

FIG. 16

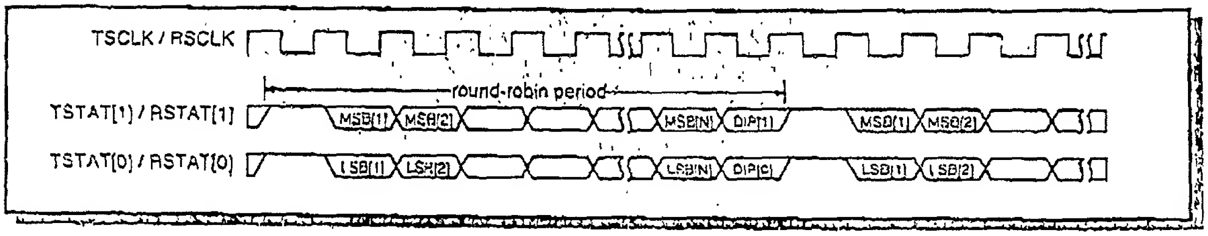

TSCLK / RSCLK
round-robin period
TSTAT[1] / RSTAT[1]
TSTAT[0] / RSTAT[0]
MSB[1]
MSB[2]
MSB[N]
DIP[1]
MSB[1]
MSB[2]
LSB[1]
LSB[2]
LSB[N]
DIP[0]
LSB[1]
LSB[2]

FIG. 17

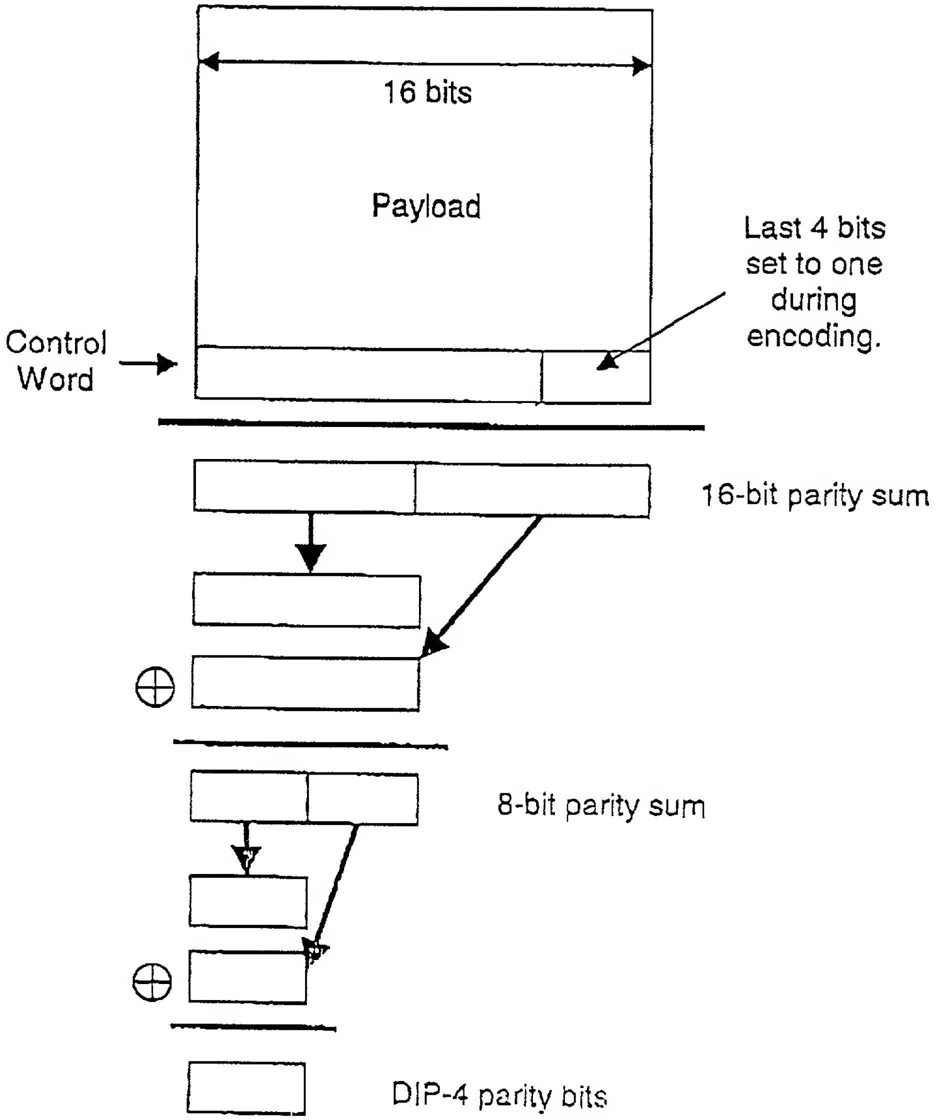

16 bits
Payload
Last 4 bits set to one during encoding.
Control Word
16-bit parity sum
⊕
8-bit parity sum
⊕
DIP-4 parity bits

FIG. 18

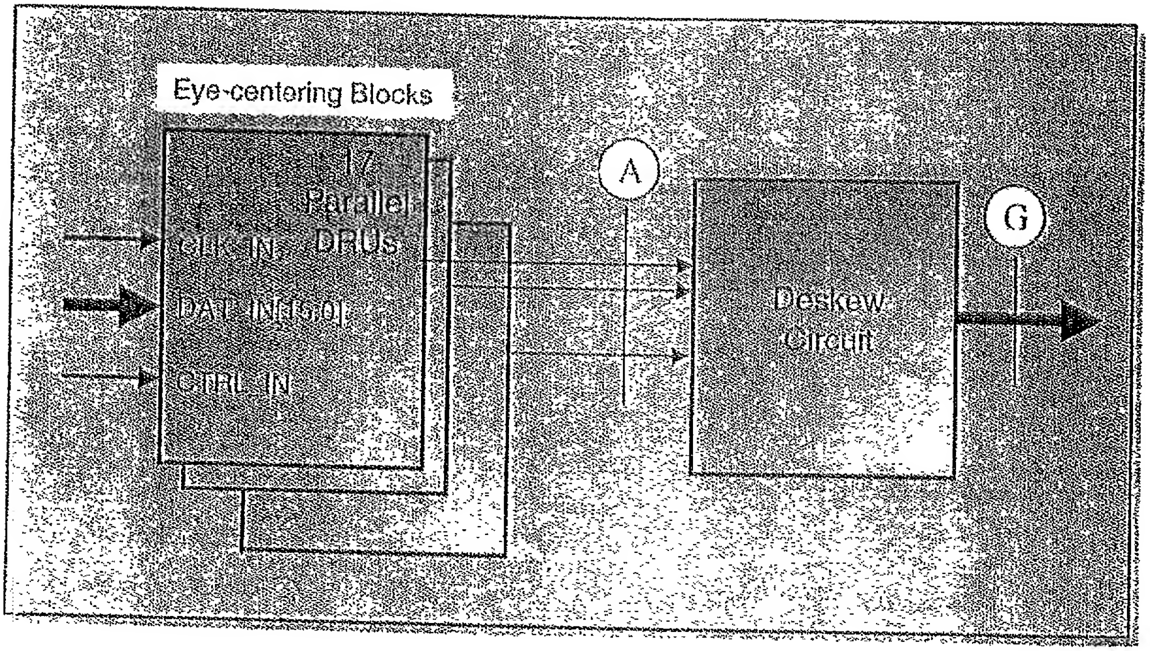

Eye-centering Blocks
17 Parallel DRUs
CLK IN
DAT_IN[15:0]
CTRL_IN
A
Deskew Circuit
G

FIG. 19

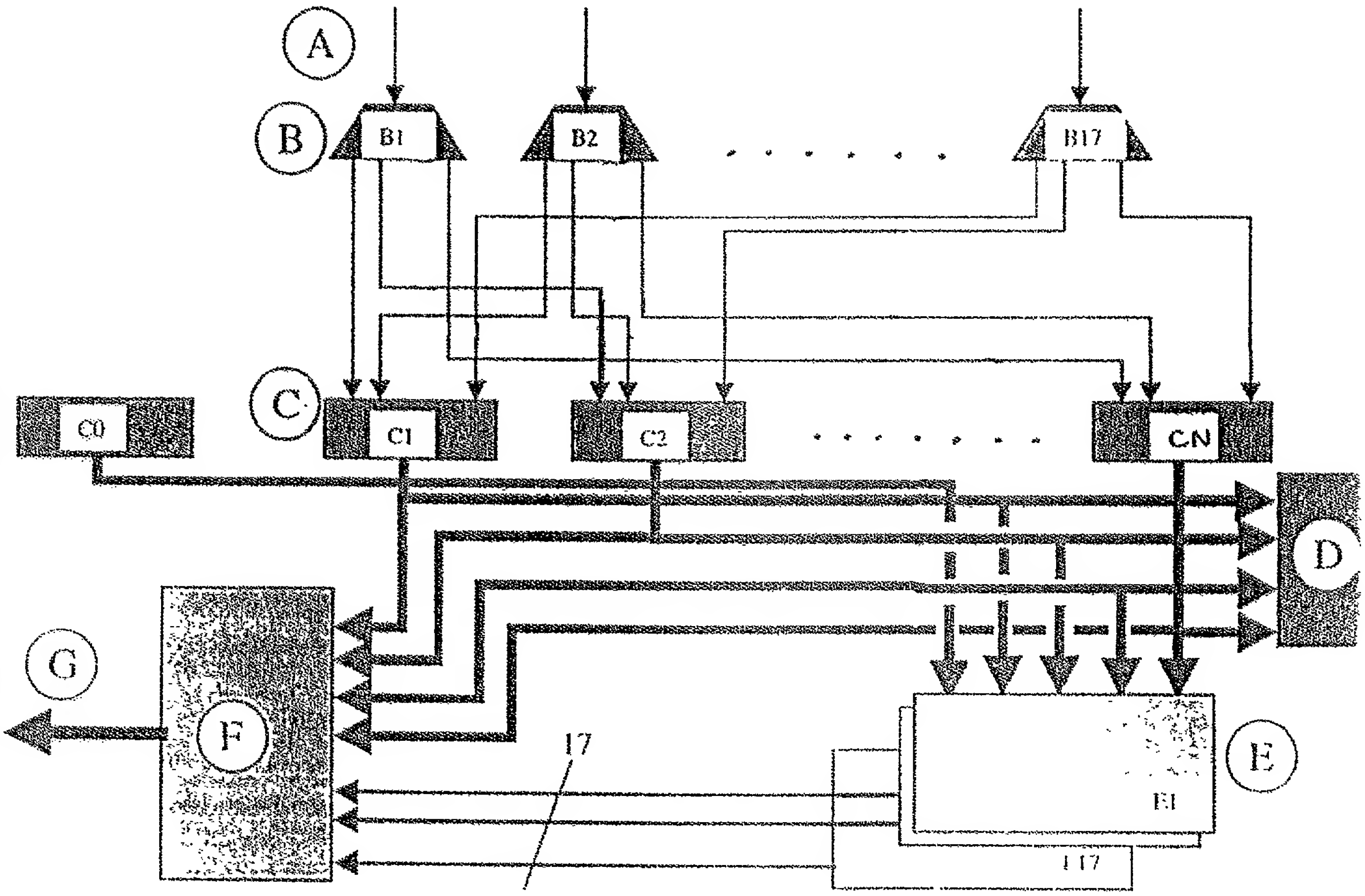
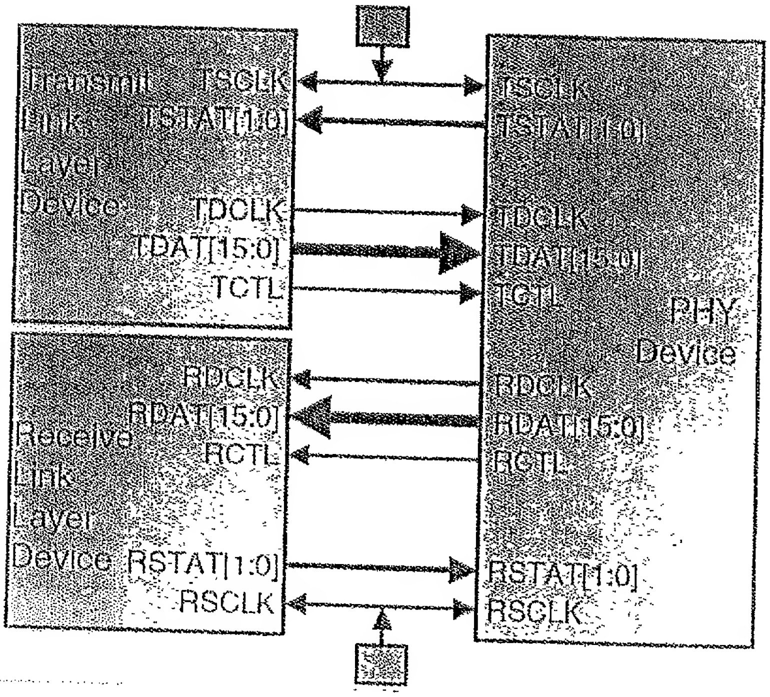


FIG. 20


Transmit Link Layer Device
TSCLK
TSTAT[1:0]
TDCLK
TDAT[15:0]
TCTL
Receive Link Layer Device
RDCLK
RDAT[15:0]
RCTL
RSTAT[1:0]
RSCLK
TSCLK
TSTAT[1:0]
TDCLK
TDAT[15:0]
TCTL
PHY Device
RDCLK
RDAT[15:0]
RCTL
RSTAT[1:0]
RSCLK